UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,742	10/01/2004	Dale W. Martin	BUR920040053US1	5741

30449 7590 01/25/2006

SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,742	MARTIN ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 13-20* is/are rejected.

7)☒ Claim(s) *4 and 6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed 11/03/2005.

Currently, claims 1-20 are pending. Claims 9-12 are withdrawn from consideration.

Election/Restrictions

1. Applicant's election of 1-8 and 13-20 in the reply filed on 11/03/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 9-12 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/03/2005.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Parat et al. (U.S. Patent No. 6,194,784 dated 2/27/2001) in view of Park et al. (U.S. Publication No. 2005/0048732 filed 8/26/2003) .

Parat shows the method as substantially claimed in Figs. 1-12 and corresponding text as: providing a semiconductor region (210); forming a gate stack on top of the semiconductor region, the gate stack including: a gate dielectric region (231) on top of the semiconductor region (col. 5, lines 5-30), a first gate polysilicon region (232) on top of the gate dielectric region (col. 5, lines 5-30), a second gate polysilicon (230) region on top of the first gate polysilicon region (col. 5, lines 5-30), the second gate polysilicon region being doped with a type of dopants (col. 5, lines 5-30); and forming on a side wall of the gate stack a diffusion barrier region (237) (protective layer) and a spacer region (238) (col. 5, lines 45-59), wherein the diffusion barrier region is sandwiched between the gate stack and the spacer region, and wherein the diffusion barrier region is in direct physical contact with both the first and second polysilicon regions (col. 5, lines 45-59) (claim 1). Parat teaches that the second gate polysilicon region is doped with n-type dopants (col. 5, lines 5-30) (claim 2). Parat teaches the formation of a gate dielectric

layer on top of the semiconductor region; forming a gate polysilicon layer on top of the gate dielectric layer; implanting the type of dopants into a top layer of the gate polysilicon layer; and etching away portions of the gate polysilicon layer and the gate dielectric layer such that what remains of the gate polysilicon layer after the step of etching comprises the first and second polysilicon regions, and what and what remains of the gate dielectric layer after the step of etching comprises the gate dielectric region (col. 5, lines 5-30) (claim 3). Parat teaches the forming of the diffusion barrier region at a top surface of the side wall of the gate stack (col. 5, lines 45-59); and forming the spacer region on top of the diffusion barrier region after the step of forming the diffusion barrier region (col. 5, lines 45-59) (claim 5).

Parat shows the method as substantially claimed in Figs. 1-12 and corresponding text as: providing a semiconductor region (210); forming a gate stack on top of the semiconductor region, the gate stack including: a gate dielectric region (231) on top of the semiconductor region (col. 5, lines 5-30), a first gate polysilicon region (232) on top of the gate dielectric region (col. 5, lines 5-30), a second gate polysilicon (230) region on top of the first gate polysilicon region (col. 5, lines 5-30), the second gate polysilicon region being doped with a type of dopants (col. 5, lines 5-30); and forming on first and second side walls of the gate stack first and second diffusion barrier region (237) (protective layer) and first and second spacer region (238) (col. 5, lines 45-59), wherein the first diffusion barrier region is sandwiched between the gate stack and the first spacer region, and wherein the first diffusion barrier region is in direct physical contact with both the first and second polysilicon regions (col. 5, lines 45-59), wherein the

second diffusion barrier region is sandwiched between the gate stack and the second spacer region, and wherein the second diffusion barrier region is in direct physical contact with both the first and second polysilicon regions (col. 5, lines 45-59) (claim 13). Parat teaches that the second gate polysilicon region is doped with n-type dopants (col. 5, lines 5-30) (claim 14). Parat teaches the formation of a gate dielectric layer on top of the semiconductor region; forming a gate polysilicon layer on top of the gate dielectric layer; implanting the type of dopants into a top layer of the gate polysilicon layer; and etching away portions of the gate polysilicon layer and the gate dielectric layer such that what remains of the gate polysilicon layer after the step of etching comprises the first and second polysilicon regions, and what and what remains of the gate dielectric layer after the step of etching comprises the gate dielectric region (col. 5, lines 5-30) (claim 15). Parat teaches the forming of the diffusion barrier region at a top surface of the side wall of the gate stack (col. 5, lines 45-59); and forming the spacer region on top of the diffusion barrier region after the step of forming the diffusion barrier region (col. 5, lines 45-59) (claim 17).

Parat lacks anticipation only in not explicitly teaching that: 1) forming on the side wall of the gate stack diffusion barrier regions and spacer oxide regions (claims 1 and 13).

Park discloses the formation of a barrier layer around a gate stack. Park teaches a protective cap (30) is formed over the structure layer (30) is formed as a nitride layer [0038]. Park teaches that oxide spacers (60) are then formed over the protective cap

(30)[0043]. These procedures are done to stabilize the parasitic capacitance between the gate and the source and drain. [0003].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Parat by, forming a diffusion barrier region and an oxide spacer, as taught by Park, with the motivation, that Park teaches the stabilization of the parasitic capacitance between the gate and the source and drain.

Double Patenting

7. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

8. Claims 13-20 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 1-8. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

9. Claims 4 and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
January 19, 2006